Description

The HR4982 is a complete microstepping motor driver with built-in translator for easy operation. It is designed to operate bipolar stepper motors in full-,1/8-, 1/16- and 1/128- step modes, with an output drive capacity of up to 35 V and ± 2 A. The HR4982 includes a fixed off-time current regulator which has the ability to operate in Slow or Mixed decay modes.

The translator is the key to the easy implementation of the HR4982. Simply inputting one pulse on the STEP input drives the motor one microstep. There are no phase sequence tables, high frequency control lines, or complex interfaces to program. The HR4982 interface is an ideal fit for applications where a complex microprocessor is unavailable or is overburdened.

During stepping operation, the chopping control in the HR4982 automatically selects the current decay mode, Slow or Mixed. In Mixed decay mode, the device is set initially to a fast decay for a proportion of the fixed off-time, then to a slow decay for the remainder of the off-time. Mixed decay current control results in reduced audible motor noise, increased step accuracy, and reduced power dissipation.

Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation. Internal circuit protection includes: thermal shutdown with hysteresis, undervoltage lockout (UVLO), and crossover-current protection. Special power-on sequencing is not required.

The HR4982 is supplied in a low-profile (height≤1.20mm), 28-pin TSSOP with exposed thermal pad. It is lead (Pb) free (suffix -T), with 100% matte tin plated leadframes.

Features and Benefits

- Low RDS(ON) outputs
- Automatic current decay mode detection/selection
- Mixed and Slow current decay modes
- Synchronous rectification for low power dissipation
- Internal UVLO
- Crossover-current protection
- 3.3 and 5 V compatible logic supply
- Thermal shutdown circuitry
- Short-to-ground protection
- Shorted load protection
- Four selectable step modes: full, 1/8, 1/16, and 1/128

Package



24 lead TSSOP (suffix LP) with exposed thermal pad

Selection Guide

]	Part Number	Package
]	HR4982	TSSOP24 with exposed thermal pad





Typical Application Diagram

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Load Supply Voltage	V _{BB}		35	V
Output Current	I _{OUT}		±2	А
Logic Input voltage	VIN		-0.3 to 5.5	V
Logic Supply voltage	V _{DD}		-0.3 to 5.5	V
Motor Output Votage			-2.0 to 37	V
Sense Voltage	V _{SENSE}		-0.5 to 0.5	V
Reference Voltage	VREF		5.5	V
Operating Ambient Temperature	TA	Range S	-20 to 85	°C
Maximum Junction	TJ(max)		150	°C
Storage Temperature	T _{stg}		-55 to 150	°C

RECOMMENDED OPERATING CONDITIONS at Ta = 25°C

		Min	NOM	Max	Unit
Load Supply Voltage	VBB	8	-	35	V
Logic Supply voltage	VCC	3	-	5.5	V
Output Current	IOUT	0		1.8	Α

RECOMMENDED SETTING:

- 1. ROSC: For 1/128 microstep recommend choose $10k\Omega$ to $15k\Omega$ ROSC.
 - If necessary please choose the suitable ROSC resistance according motor
 - and the control frequency.
 - $t_{OFF} \cong R_{OSC}/825$, the unit of $t_{OFF}\,is\,us\,{}_{\circ}$
 - For 1/16 microstep, you can just connect the ROSC pin to GND, lead to the toff=30us.
- 2、 CP capacity: 0.1uF/50V
- **3** VCP capacity: 0.1uF/50V
- **4** VREG capacity: 0.22uF/16V
- 5. VREF reference voltage, $0.8V 3V_{\odot}$
- 6. RSENSE register, according to VREF and target current, $I_{Trip MAX} = VREF / (8 \times Rs)$
 - According to target current, choose the Rsense, make the value

Vsense = Imax * Rsense between 0.35V to 0.45V. Then choose the Vref according

 $Vref = 8 * Vsense. 8 \times Rs$



ELECTRICAL CHARACTERISTICS¹ at Ta = 25°C, V_{BB}= 35 V Min Typ² Unit Parameter Symbol Conditions Max **Output Drivers** V 8 Load Supply Voltage Range V_{BB} Operating 35 3.0 V Logic Supply Voltage Range VDD Operating _ 5.5 430 Output On Resistance Source Driver, Iout=-1.5A 320 mΩ RDS(ON) Sink Driver, IouT=1.5A 320 430 mΩ V Body Diode Forward Voltage Source Diode, IF=-1.5A 1.2 VF V Sink Diode, IF=1.5A 1.2 Motor Supply Current fpwm<50kHz 4 mА I_{BB} Operating, outputs disabled 2 mA Logic Supply Current fpwm<50kHz 8 mA I_{DD} 5 mA Operating, outputs disabled **Control Logic** V Logic Input Voltage VIN(1) VDD*0.7 VDD*0.3 V VIN(0) 20 Logic Input Current VIN=VDD×0.7 -20 <1.0 $I_{IN(1)}$ uA IIN(0) $V_{IN}=V_{DD}\times 0.3$ -20 <1.0 20 uA 33 Microstep Select R_{MS1} _ kΩ R_{MS2} _ 100 _ kΩ Logic Input Hysteresis As a % of VDD 5 11 19 % VHYS(IN) Blank Time 0.7 1.3 1 t_{BLANK} us Fixed Off-Time OSC=VDD or GND 20 30 40 us toff 23 30 37 $Rosc=25k\Omega$ us Reference Input Voltage Range VREF 0.5 _ 4 V Reference Input Current IREF -3 0 3 uA Current Trip-Level Error³ V_{REF}=2V,%I_{TripMAX}=38.27% ± 15 % --V_{REF}=2V,%I_{TripMAX}=70.71% ± 5 % errı _ -% VREF=2V,%ITripMAX=100% ± 5 Crossover Dead Time 100 475 800 t_{DT} ns Protection Overcurren Protection Threshold⁴ IOCPST 3 А --Thermal Shutdown Temperature TtSD 165 °C _ _ °C Thermal Shutdown Hysteresis TTSDHYS 15 _ _ V VDD Undervoltage Lockout 2.8 2.9 VDDUVLO V_{DD} rising 2.7 90 mV VDD Undervoltage Hysteresis VDDUVLOHYS _ _

1For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

2Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within

the specified maximum and minimum limits.

3VERR = [(VREF/8) - VSENSE] / (VREF/8).

4Overcurrent protection (OCP) is tested at TA = 25°C in a restricted range and guaranteed by characterization.



Timing Diagram:

 $(T_A = +25 \degree C, V_{DD} = 5 \text{ V}, \text{ logic is } V_{DD} \text{ or } \text{GND})$



Time Duration	Symbol	Тур.	Unit
STEP minimum, HIGH pulse width	t _A	1	μs
STEP minimum, LOW pulse width	t _B	1	μs
Setup time, input change to STEP	t _C	200	ns
Hold time, input change to STEP	t _D	200	ns

Figure 1: Logic Interface Timing Diagram

FF8							
MS1	MS2	Microstep Resolution	Excitation Mode				
L	L	Full Step	2 Phase				
Н	L	1/8 Step	1-2 Phase				
Н	Н	1/16 Step	8W1-2 Phase				
L	Н	1/128 Step	32W1-2 Phase				







Functional Description

Device Operation. The HR4982 is a complete microstepping motor driver with a built-in translator for easy operation with minimal control lines. It is designed to operate bipolar stepper motors in full-, 1/8-, 1/16-, and 1/128-step modes. The currents in each of the two output full-bridges and all of the N-channel DMOS FETs are regulated with fixed off-time PWM (pulse width modulated) control circuitry. At each step, the current for each full-bridge is set by the value of its external current-sense resistor (RS1 and RS2), a reference voltage (VREF), and the output voltage of its DAC (which in turn is controlled by the output of the translator).

At power-on or reset, the translator sets the DACs and the phase current polarity to the initial Home state, and the current regulator to Mixed Decay Mode for both phases. When a step command signal occurs on the STEP input, the translator automatically sequences the DACs to the next level and current polarity. The microstep resolution is set by the combined effect of the MSx inputs, as shown in Table 1.

When stepping, if the new output levels of the DACs are lower than their previous output levels, then the decay mode for the active full-bridge is set to Mixed. If the new output levels of the DACs are higher than or equal to their previous levels, then the decay mode for the active full-bridge is set to Slow. This automatic current decay selection improves microstepping performance by reducing the distortion of the current waveform that results from the back EMF of the motor.

Microstep Select (MSx). The microstep resolution is set by the voltage on logic inputs MSx, as shown in Table 1. The MS1 and MS2 pins have a 100 k Ω pull-down resistance. When changing the step mode the change does not take effect until the next STEP rising edge.

If the step mode is changed without a translator reset, and absolute position must be maintained, it is important to change the step mode at a step position that is common to both step modes in order to avoid missing steps. When the device is powered down, or reset due to TSD or an over current event the translator is set to the home position which is by default common to all step modes. **Mixed Decay Operation.** The bridge operates in Mixed decay mode, at power-on and reset, and during normal running according to the ROSC configuration and the step sequence. During Mixed decay, when the trip point is reached, the HR4982 initially goes into a fast decay mode for 31.25% of the off-time, torF . After that, it switches to Slow decay mode for the remainder of torF. A timing diagram for this feature appears on figure 7.

Typically, mixed decay is only necessary when the current in the winding is going from a higher value to a lower value as determined by the state of the translator. For most loads automatically-selected mixed decay is convenient because it minimizes ripple when the current is rising and prevents missed steps when the current is falling. For some applications where microstepping at very low speeds is necessary, the lack of back EMF in the winding causes the current to increase in the load quickly, resulting in missed steps. This is shown in Figure 2. By pulling the ROSC pin to ground, mixed decay is set to be active 100% of the time, for both rising and falling currents, and prevents missed steps as shown in Figure 3. If this is not an issue, it is recommended that automatically-selected mixed decay be used, because it will produce reduced ripple currents. Refer to the Fixed Off-Time section for details.

Low Current Microstepping. Intended for applications where the minimum on-time prevents the output current from regulating to the programmed current level at low current steps. To prevent this, the device can be set to operate in Mixed decay mode on both rising and falling portions of the current waveform. This feature is implemented by shorting the ROSC pin to ground. In this state, the off-time is internally set to 30 µs.

Reset Input (RESET). The RESET input sets the translator to a predefined Home state, and turns off all of the FET outputs. All STEP inputs are ignored until the RESET input is set to high.

Step Input (STEP). A low-to-high transition on the STEP input sequences the translator and advances the motor one increment. The translator controls the input to the DACs and the direction of current flow in each winding. The size of the increment is determined by the combined state of the MSx inputs.



Direction Input (DIR). This determines the direction of rotation of the motor. Changes to this input do not take effect until the next STEP rising edge.

Internal PWM Current Control. Each full-bridge is controlled by a fixed off-time PWM current control circuit that limits the load current to a desired value, ITRIP . Initially, a diagonal pair of source and sink FET outputs are enabled and current flows through the motor winding and the current sense resistor, RSx. When the voltage across RSx equals the DAC output voltage, the current sense comparator resets the PWM latch. The latch then turns off the appropriate source driver and initiates a fixed off time decay mode

The maximum value of current limiting is set by the selection of RSx and the voltage at the VREF pin. The transconductance function is approximated by the maximum value of current limiting, ITripMAX (A), which is set by

 $ITripMAX = VREF / (8 \times Rs)$

where RS is the resistance of the sense resistor (Ω) and VREF is the input voltage on the REF pin (V).

The DAC output reduces the VREF output to the current sense comparator in precise steps, such that

Itrip = (%I_{TripMAX} / 100) × I_{TripMAX}

(See Table 2 for %ITripMAX at each step.)

It is critical that the maximum rating (0.5 V) on the SENSE1 and SENSE2 pins is not exceeded.

Fixed Off-Time. The internal PWM current control circuitry uses a one-shot circuit to control the duration of time that the DMOS FETs remain off. The off-time, toFF, is determined by the ROSC terminal. ROSC terminal has three settings:

 ROSC tied to VDD — off-time internally set to 30 µs, decay mode is automatic Mixed decay except when in full step where decay mode is set to Slow decay.

ROSC tied directly to ground — off-time internally set to 30 µs, current decay is set to Mixed decay for both increasing and decreasing currents for all step modes.

• ROSC through a resistor to ground — off-time is determined by the following formula, the decay mode is automatic Mixed decay for all step modes except full step whic is set to slow decay.

toff $\approx ROSC / 825$

Where toFF is in µs.

Blanking. This function blanks the output of the current sense comparators when the outputs are switched by the internal current control circuitry. The comparator outputs are blanked to prevent false overcurrent detection due to reverse recovery currents of the clamp diodes, and switching transients related to the capacitance of the load. The blank time, tBLANK (µs), is approximately

$t_{\text{blank}} \approx 1 \ \mu s$

Shorted-Load and Short-to-Ground

Protection. If the motor leads are shorted together, or if one of the leads is shorted to ground, the driver will protect itself by sensing the overcurrent event and disabling the driver that is shorted, protecting the device from damage. In the case of a short-to-ground, the device will remain disabled (latched) until the SLEEP input goes high or VDD power is removed. A short-to-ground overcurrent event is shown in Figure 4. When the two outputs are shorted together, the current path is through the sense resistor. After the blanking time ($\approx 1 \ \mu s$) expires, the sense resistor voltage is exceeding its trip value, due to the overcurrent condition that exists. This causes the driver to go into a fixed off-time cycle. After the fixed off-time expires the driver turns on again and the process repeats. In this condition the driver is completely protected against overcurrent events, but the short is repetitive with a period equal to the fixed off-time of the driver. This condition is shown in Figure 5.

During a shorted load event it is normal to observe both a positive and negative current spike as shown in Figure 3, due to the direction change implemented by the Mixed decay feature. This is shown in Figure 6. In both instances the overcurrent circuitry is protecting the driver and prevents damage to the device.

Charge Pump (CP1 and CP2). The charge pump is used to generate a gate supply greater than that of VBB for driving the source-side FET gates. A $0.1 \,\mu\text{F}$ ceramic capacitor, should be connected between CP1 and CP2. In addition, a $0.1 \,\mu\text{F}$ ceramic capacitor is required between VCP and VBB, to act as a reservoir for operating the high-side FET gates.

Capacitor values should be Class 2 dielectric $\pm 15\%$ maximum, or tolerance R, according to EIA (Electronic Industries Alliance) specifications.





VREG(VREG). This internally-generated voltage is used to operate the sink-side FET outputs. The nominal output voltage of the VREG terminal is 5.5 V. The VREG pin must be decoupled with a 0.22 μ F ceramic capacitor to ground. VREG is internally monitored. In the case of a fault condition, the FET outputs of the HR4982 are disabled.

Capacitor values should be Class 2 dielectric $\pm 15\%$ maximum, or tolerance R, according to EIA (Electronic Industries Alliance) specifications.

Enable Input (ENABLE). This input turns on or off all of the FET outputs. When set to a logic high, the outputs are disabled. When set to a logic low, the internal control enables the outputs as required. The translator inputs STEP, DIR, and MSx, as well as the internal sequencing logic, all remain active, independent of the ENABLE input state.

Shutdown. In the event of a fault, overtemperature (excess TJ) or an undervoltage (on VCP), the FET outputs of the HR4982 are disabled until the fault condition is removed. At power-on, the UVLO (undervoltage lockout) circuit disables the FET outputs and resets the translator to the Home state.

Sleep Mode (SLEEP). To minimize power consumption when the motor is not in use, this input disables much of the internal circuitry including the output FETs, current regulator, and charge pump. A logic low on the SLEEP pin puts the HR4982 into Sleep mode. A logic high allows normal operation, as well as start-up (at which time the HR4982 drives the motor to the Home microstep position). When emerging from Sleep mode, in order to allow the charge pump to stabilize, provide a delay of 1 ms before issuing a Step command.

Synchronous Rectification. When a PWM-off cycle is triggered by an internal fixed-off time cycle, load current recirculates according to the decay mode selected by the control logic. This synchronous rectification feature turns on the appropriate FETs during current decay, and effectively shorts out the body diodes with the low FET RDS(ON). This reduces power dissipation significantly, and can eliminate the need for external Schottky diodes in many applications. Synchronous rectification turns off when the load current approaches zero (0 A), preventing reversal of the load current.







Symbol	Characteristic					
t _{off}	Device fixed off-time					
IPEAK	Maximum output current					
t _{SD}	Slow decay interval					
t _{FD}	Fast decay interval					
I _{OUT}	Device output current					

Figure 7: Current Decay Modes Timing Chart



Application Layout

Layout. The printed circuit board should use a heavy groundplane. For optimum electrical and thermal performance, the HR4982 must be soldered directly onto the board. Pins 3 and 18 are internally fused, which provides a path for enhanced thermal dissipation. Theses pins should be soldered directly to an exposed surface on the PCB that connects to thermal vias are used to transfer heat to other layers of the PCB.

In order to minimize the effects of ground bounce and offset issues, it is important to have a low impedance single-point ground, known as a *star ground*, located very close to the device. By making the connection between the pad and the ground plane directly under the HR4982, that area becomes an ideal location for a star ground point. A low impedance ground will prevent ground bounce during high current operation and ensure that the supply voltage remains stable at the input terminal.

The two input capacitors should be placed in parallel, and as close to the device supply pins as possible. The ceramic capacitor (CIN1) should be closer to the pins than the bulk capacitor (CIN2). This is necessary because the ceramic capacitor will be responsible for delivering the high frequency current components. The sense resistors, RSx , should have a very low impedance path to ground, because they must carry a large current while supporting very accurate voltage measurements by the current sense comparators. Long ground traces will cause additional voltage drops, adversely affecting the ability of the comparators to accurately measure the current in the windings. The SENSEx pins have very short traces to the RSx resistors and very thick, low impedance traces directly to the star ground underneath the device. If possible, there should be no other components on the sense circuits.









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Pin Circuit Diagrams

Decay Modes for Eighth-Step Increments



Table 2: Step Sequencing Settings

Home microstep position at Step Angle 45°; DIR = H

1/128	1/16	1/8	full	Phase 1 Current	Phase 2 Current	Step Angle
				[% ItripMax] (%)	[% ItripMax] (%)	(°)
1	1	1		100.0	0.0	0.00
2				100.0	1.2	0.70
3				100.0	2.5	1.41
4				99.9	3.7	2.11
5				99.9	4.9	2.81
6				99.8	6.1	3.52
7				99.7	7.4	4.22
8				99.6	8.6	4.92
9	2			99.5	9.8	5.63
10				99.4	11.0	6.33
11				99.2	12.2	7.03
12				99.1	13.5	7.73
13				98.9	14.7	8.44
14				98.7	15.9	9.14
15				98.5	17.1	9.84
16				98.3	18.3	10.55
17	3	2		98.1	19.5	11.25
18				97.8	20.7	11.95
19				97.6	21.9	12.66
20				97.3	23.1	13.36
21				97.0	24.3	14.06
22				96.7	25.5	14.77
23				96.4	26.7	15.47
24				96.0	27.9	16.17
25	4			95.7	29.0	16.88
26				95.3	30.2	17.58
27				95.0	31.4	18.28
28				94.6	32.5	18.98
29				94.2	33.7	19.69
30				93.7	34.8	20.39
31				93.3	36.0	21.09
32				92.9	37.1	21.80
33	5	3		92.4	38.3	22.50
34				91.9	39.4	23.20
35				91.4	40.5	23.91
36				90.9	41.6	24.61
37				90.4	42.8	25.31
38				89.9	43.9	26.02
39				89.3	45.0	26.72



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				-		
40				88.8	46.1	27.42
41	6			88.2	47.1	28.13
42				87.6	48.2	28.83
43				87.0	49.3	29.53
44				86.4	50.4	30.23
45				85.8	51.4	30.94
46				85.1	52.5	31.64
47				84.5	53.5	32.34
48				83.8	54.5	33.05
49	7	4		83.1	55.6	33.75
50				82.5	56.6	34.45
51				81.8	57.6	35.16
52				81.0	58.6	35.86
53				80.3	59.6	36.56
54				79.6	60.6	37.27
55				78.8	61.5	37.97
56				78.1	62.5	38.67
57	8			77.3	63.4	39.38
58				76.5	64.4	40.08
59				75.7	65.3	40.78
60				74.9	66.2	41.48
61				74.1	67.2	42.19
62				73.3	68.1	42.89
63				72.4	69.0	43.59
64				71.6	69.8	44.30
65	9	5	1	70.7	70.7	45.00
66				69.8	71.6	45.70
67				69.0	72.4	46.41
68				68.1	73.3	47.11
69				67.2	74.1	47.81
70				66.2	74.9	48.52
71				65.3	75.7	49.22
72				64.4	76.5	49.92
73	10			63.4	77.3	50.63
74				62.5	78.1	51.33
75				61.5	78.8	52.03
76				60.6	79.6	52.73
77				59.6	80.3	53.44
78				58.6	81.0	54.14
79				57.6	81.8	54.84
80				56.6	82.5	55.55
81	11	6		55.6	83.1	56.25
82				54.5	83.8	56.95
83				53.5	84.5	57.66
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84			52.5	85.1	58.36
85			51.4	85.8	59.06
86			50.4	86.4	59.77
87			49.3	87.0	60.47
88			48.2	87.6	61.17
89	12		47.1	88.2	61.88
90			46.1	88.8	62.58
91			45.0	89.3	63.28
92			43.9	89.9	63.98
93			42.8	90.4	64.69
94			41.6	90.9	65.39
95			40.5	91.4	66.09
96			39.4	91.9	66.80
97	13	7	38.3	92.4	67.50
98			37.1	92.9	68.20
99			36.0	93.3	68.91
100			34.8	93.7	69.61
101			33.7	94.2	70.31
102			32.5	94.6	71.02
103			31.4	95.0	71.72
104			30.2	95.3	72.42
105	14		29.0	95.7	73.13
106			27.9	96.0	73.83
107			26.7	96.4	74.53
108			25.5	96.7	75.23
109			24.3	97.0	75.94
110			23.1	97.3	76.64
111			21.9	97.6	77.34
112			20.7	97.8	78.05
113	15	8	19.5	98.1	78.75
114			18.3	98.3	79.45
115			17.1	98.5	80.16
116			15.9	98.7	80.86
117			14.7	98.9	81.56
118			13.5	99.1	82.27
119			12.2	99.2	82.97
120			11.0	99.4	83.67
121	16		9.8	99.5	84.38
122			8.6	99.6	85.08
123			7.4	99.7	85.78
124			6.1	99.8	86.48
125			4.9	99.9	87.19
126			3.7	99.9	87.89
127			2.5	100.0	88.59
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128			1.2	100.0	89.30
129	17	9	0.0	100.0	90.00
130			-1.2	100.0	90.70
131			-2.5	100.0	91.41
132			-3.7	99.9	92.11
133			-4.9	99.9	92.81
134			-6.1	99.8	93.52
135			-7.4	99.7	94.22
136			-8.6	99.6	94.92
137	18		-9.8	99.5	95.63
138			-11.0	99.4	96.33
139			-12.2	99.2	97.03
140			-13.5	99.1	97.73
141			-14.7	98.9	98.44
142			-15.9	98.7	99.14
143			-17.1	98.5	99.84
144			-18.3	98.3	100.55
145	19	10	-19.5	98.1	101.25
146			-20.7	97.8	101.95
147			-21.9	97.6	102.66
148			-23.1	97.3	103.36
149			-24.3	97.0	104.06
150			-25.5	96.7	104.77
151			-26.7	96.4	105.47
152			-27.9	96.0	106.17
153	20		-29.0	95.7	106.88
154			-30.2	95.3	107.58
155			-31.4	95.0	108.28
156			-32.5	94.6	108.98
157			-33.7	94.2	109.69
158			-34.8	93.7	110.39
159			-36.0	93.3	111.09
160			-37.1	92.9	111.80
161	21	11	-38.3	92.4	112.50
162			-39.4	91.9	113.20
163			-40.5	91.4	113.91
164			-41.6	90.9	114.61
165			-42.8	90.4	115.31
166			-43.9	89.9	116.02
167			-45.0	89.3	116.72
168			-46.1	88.8	117.42
169	22		-47.1	88.2	118.13
170			-48.2	87.6	118.83
171			-49.3	87.0	119.53
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172				-50.4	86.4	120.23
173				-51.4	85.8	120.94
174				-52.5	85.1	121.64
175				-53.5	84.5	122.34
176				-54.5	83.8	123.05
177	23	12		-55.6	83.1	123.75
178				-56.6	82.5	124.45
179				-57.6	81.8	125.16
180				-58.6	81.0	125.86
181				-59.6	80.3	126.56
182				-60.6	79.6	127.27
183				-61.5	78.8	127.97
184				-62.5	78.1	128.67
185	24			-63.4	77.3	129.38
186				-64.4	76.5	130.08
187				-65.3	75.7	130.78
188				-66.2	74.9	131.48
189				-67.2	74.1	132.19
190				-68.1	73.3	132.89
191				-69.0	72.4	133.59
192				-69.8	71.6	134.30
193	25	13	2	-70.7	70.7	135.00
194				-71.6	69.8	135.70
195				-72.4	69.0	136.41
196				-73.3	68.1	137.11
197				-74.1	67.2	137.81
198				-74.9	66.2	138.52
199				-75.7	65.3	139.22
200				-76.5	64.4	139.92
201	26			-77.3	63.4	140.63
202				-78.1	62.5	141.33
203				-78.8	61.5	142.03
204				-79.6	60.6	142.73
205				-80.3	59.6	143.44
206				-81.0	58.6	144.14
207				-81.8	57.6	144.84
208				-82.5	56.6	145.55
209	27	14		-83.1	55.6	146.25
210				-83.8	54.5	146.95
211				-84.5	53.5	147.66
212				-85.1	52.5	148.36
213				-85.8	51.4	149.06
214				-86.4	50.4	149.77
215				-87.0	49.3	150.47
ronic To		-				

Jiaxing Heroic Electronic Technology Co., Ltd.



HR4982

216			-87.6	48.2	151.17
217	28		-88.2	47.1	151.88
218			-88.8	46.1	152.58
219			-89.3	45.0	153.28
220			-89.9	43.9	153.98
221			-90.4	42.8	154.69
222			-90.9	41.6	155.39
223			-91.4	40.5	156.09
224			-91.9	39.4	156.80
225	29	15	-92.4	38.3	157.50
226			-92.9	37.1	158.20
227			-93.3	36.0	158.91
228			-93.7	34.8	159.61
229			-94.2	33.7	160.31
230			-94.6	32.5	161.02
231			-95.0	31.4	161.72
232			-95.3	30.2	162.42
233	30		-95.7	29.0	163.13
234			-96.0	27.9	163.83
235			-96.4	26.7	164.53
236			-96.7	25.5	165.23
237			-97.0	24.3	165.94
238			-97.3	23.1	166.64
239			-97.6	21.9	167.34
240			-97.8	20.7	168.05
241	31	16	-98.1	19.5	168.75
242			-98.3	18.3	169.45
243			-98.5	17.1	170.16
244			-98.7	15.9	170.86
245			-98.9	14.7	171.56
246			-99.1	13.5	172.27
247			-99.2	12.2	172.97
248			-99.4	11.0	173.67
249	32		-99.5	9.8	174.38
250			-99.6	8.6	175.08
251			-99.7	7.4	175.78
252			-99.8	6.1	176.48
253			-99.9	4.9	177.19
254			-99.9	3.7	177.89
255			-100.0	2.5	178.59
256			-100.0	1.2	179.30
257	33	17	-100.0	0.0	180.00
258			-100.0	-1.2	180.70
259			-100.0	-2.5	181.41
ronic To	- 1 1 -				

Jiaxing Heroic Electronic Technology Co., Ltd.



HR4982

260			-99.9	-3.7	182.11
261			-99.9	-4.9	182.81
262			-99.8	-6.1	183.52
263			-99.7	-7.4	184.22
264			-99.6	-8.6	184.92
265	34		-99.5	-9.8	185.63
266			-99.4	-11.0	186.33
267			-99.2	-12.2	187.03
268			-99.1	-13.5	187.73
269			-98.9	-14.7	188.44
270			-98.7	-15.9	189.14
271			-98.5	-17.1	189.84
272			-98.3	-18.3	190.55
273	35	18	-98.1	-19.5	191.25
274			-97.8	-20.7	191.95
275			-97.6	-21.9	192.66
276			-97.3	-23.1	193.36
277			-97.0	-24.3	194.06
278			-96.7	-25.5	194.77
279			-96.4	-26.7	195.47
280			-96.0	-27.9	196.17
281	36		-95.7	-29.0	196.88
282			-95.3	-30.2	197.58
283			-95.0	-31.4	198.28
284			-94.6	-32.5	198.98
285			-94.2	-33.7	199.69
286			-93.7	-34.8	200.39
287			-93.3	-36.0	201.09
288			-92.9	-37.1	201.80
289	37	19	-92.4	-38.3	202.50
290			-91.9	-39.4	203.20
291			-91.4	-40.5	203.91
292			-90.9	-41.6	204.61
293			-90.4	-42.8	205.31
294			-89.9	-43.9	206.02
295			-89.3	-45.0	206.72
296			-88.8	-46.1	207.42
297	38		-88.2	-47.1	208.13
298			-87.6	-48.2	208.83
299			-87.0	-49.3	209.53
300			-86.4	-50.4	210.23
301			-85.8	-51.4	210.94
302			-85.1	-52.5	211.64
303			-84.5	-53.5	212.34
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HR4982

304				-83.8	-54.5	213.05
305	39	20		-83.1	-55.6	213.75
306				-82.5	-56.6	214.45
307				-81.8	-57.6	215.16
308				-81.0	-58.6	215.86
309				-80.3	-59.6	216.56
310				-79.6	-60.6	217.27
311				-78.8	-61.5	217.97
312				-78.1	-62.5	218.67
313	40			-77.3	-63.4	219.38
314				-76.5	-64.4	220.08
315				-75.7	-65.3	220.78
316				-74.9	-66.2	221.48
317				-74.1	-67.2	222.19
318				-73.3	-68.1	222.89
319				-72.4	-69.0	223.59
320				-71.6	-69.8	224.30
321	41	21	3	-70.7	-70.7	225.00
322				-69.8	-71.6	225.70
323				-69.0	-72.4	226.41
324				-68.1	-73.3	227.11
325				-67.2	-74.1	227.81
326				-66.2	-74.9	228.52
327				-65.3	-75.7	229.22
328				-64.4	-76.5	229.92
329	42			-63.4	-77.3	230.63
330				-62.5	-78.1	231.33
331				-61.5	-78.8	232.03
332				-60.6	-79.6	232.73
333				-59.6	-80.3	233.44
334				-58.6	-81.0	234.14
335				-57.6	-81.8	234.84
336				-56.6	-82.5	235.55
337	43	22		-55.6	-83.1	236.25
338				-54.5	-83.8	236.95
339				-53.5	-84.5	237.66
340				-52.5	-85.1	238.36
341				-51.4	-85.8	239.06
342				-50.4	-86.4	239.77
343				-49.3	-87.0	240.47
344				-48.2	-87.6	241.17
345	44			-47.1	-88.2	241.88
346				-46.1	-88.8	242.58
347				-45.0	-89.3	243.28
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Jiaxing Heroic Electronic Technology Co., Ltd.



HR4982

348			-43.9	-89.9	243.98
349			-42.8	-90.4	244.69
350			-41.6	-90.9	245.39
351			-40.5	-91.4	246.09
352			-39.4	-91.9	246.80
353	45	23	-38.3	-92.4	247.50
354			-37.1	-92.9	248.20
355			-36.0	-93.3	248.91
356			-34.8	-93.7	249.61
357			-33.7	-94.2	250.31
358			-32.5	-94.6	251.02
359			-31.4	-95.0	251.72
360			-30.2	-95.3	252.42
361	46		-29.0	-95.7	253.13
362			-27.9	-96.0	253.83
363			-26.7	-96.4	254.53
364			-25.5	-96.7	255.23
365			-24.3	-97.0	255.94
366			-23.1	-97.3	256.64
367			-21.9	-97.6	257.34
368			-20.7	-97.8	258.05
369	47	24	-19.5	-98.1	258.75
370			-18.3	-98.3	259.45
371			-17.1	-98.5	260.16
372			-15.9	-98.7	260.86
373			-14.7	-98.9	261.56
374			-13.5	-99.1	262.27
375			-12.2	-99.2	262.97
376			-11.0	-99.4	263.67
377	48		-9.8	-99.5	264.38
378			-8.6	-99.6	265.08
379			-7.4	-99.7	265.78
380			-6.1	-99.8	266.48
381			-4.9	-99.9	267.19
382			-3.7	-99.9	267.89
383			-2.5	-100.0	268.59
384			-1.2	-100.0	269.30
385	49	25	0.0	-100.0	270.00
386			1.2	-100.0	270.70
387			2.5	-100.0	271.41
388			3.7	-99.9	272.11
389			4.9	-99.9	272.81
390			6.1	-99.8	273.52
391			7.4	-99.7	274.22
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HR4982

392			8.6	-99.6	274.92
393	50		9.8	-99.5	275.63
394			11.0	-99.4	276.33
395			12.2	-99.2	277.03
396			13.5	-99.1	277.73
397			14.7	-98.9	278.44
398			15.9	-98.7	279.14
399			17.1	-98.5	279.84
400			18.3	-98.3	280.55
401	51	26	19.5	-98.1	281.25
402			20.7	-97.8	281.95
403			21.9	-97.6	282.66
404			23.1	-97.3	283.36
405			24.3	-97.0	284.06
406			25.5	-96.7	284.77
407			26.7	-96.4	285.47
408			27.9	-96.0	286.17
409	52		29.0	-95.7	286.88
410			30.2	-95.3	287.58
411			31.4	-95.0	288.28
412			32.5	-94.6	288.98
413			33.7	-94.2	289.69
414			34.8	-93.7	290.39
415			36.0	-93.3	291.09
416			37.1	-92.9	291.80
417	53	27	38.3	-92.4	292.50
418			39.4	-91.9	293.20
419			40.5	-91.4	293.91
420			41.6	-90.9	294.61
421			42.8	-90.4	295.31
422			43.9	-89.9	296.02
423			45.0	-89.3	296.72
424			46.1	-88.8	297.42
425	54		47.1	-88.2	298.13
426			48.2	-87.6	298.83
427			49.3	-87.0	299.53
428			50.4	-86.4	300.23
429			51.4	-85.8	300.94
430			52.5	-85.1	301.64
431			53.5	-84.5	302.34
432			54.5	-83.8	303.05
433	55	28	55.6	-83.1	303.75
434			56.6	-82.5	304.45
435			57.6	-81.8	305.16
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HR4982

436				58.6	-81.0	305.86
437				59.6	-80.3	306.56
438				60.6	-79.6	307.27
439				61.5	-78.8	307.97
440				62.5	-78.1	308.67
441	56			63.4	-77.3	309.38
442				64.4	-76.5	310.08
443				65.3	-75.7	310.78
444				66.2	-74.9	311.48
445				67.2	-74.1	312.19
446				68.1	-73.3	312.89
447				69.0	-72.4	313.59
448				69.8	-71.6	314.30
449	57	29	4	70.7	-70.7	315.00
450				71.6	-69.8	315.70
451				72.4	-69.0	316.41
452				73.3	-68.1	317.11
453				74.1	-67.2	317.81
454				74.9	-66.2	318.52
455				75.7	-65.3	319.22
456				76.5	-64.4	319.92
457	58			77.3	-63.4	320.63
458				78.1	-62.5	321.33
459				78.8	-61.5	322.03
460				79.6	-60.6	322.73
461				80.3	-59.6	323.44
462				81.0	-58.6	324.14
463				81.8	-57.6	324.84
464				82.5	-56.6	325.55
465	59	30		83.1	-55.6	326.25
466				83.8	-54.5	326.95
467				84.5	-53.5	327.66
468				85.1	-52.5	328.36
469				85.8	-51.4	329.06
470				86.4	-50.4	329.77
471				87.0	-49.3	330.47
472				87.6	-48.2	331.17
473	60			88.2	-47.1	331.88
474				88.8	-46.1	332.58
475				89.3	-45.0	333.28
476				89.9	-43.9	333.98
477				90.4	-42.8	334.69
478				90.9	-41.6	335.39
479				91.4	-40.5	336.09
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480			91.9	-39.4	336.80
481	61	31	92.4	-38.3	337.50
482			92.9	-37.1	338.20
483			93.3	-36.0	338.91
484			93.7	-34.8	339.61
485			94.2	-33.7	340.31
486			94.6	-32.5	341.02
487			95.0	-31.4	341.72
488			95.3	-30.2	342.42
489	62		95.7	-29.0	343.13
490			96.0	-27.9	343.83
491			96.4	-26.7	344.53
492			96.7	-25.5	345.23
493			97.0	-24.3	345.94
494			97.3	-23.1	346.64
495			97.6	-21.9	347.34
496			97.8	-20.7	348.05
497	63	32	98.1	-19.5	348.75
498			98.3	-18.3	349.45
499			98.5	-17.1	350.16
500			98.7	-15.9	350.86
501			98.9	-14.7	351.56
502			99.1	-13.5	352.27
503			99.2	-12.2	352.97
504			99.4	-11.0	353.67
505	64		99.5	-9.8	354.38
506			99.6	-8.6	355.08
507			99.7	-7.4	355.78
508			99.8	-6.1	356.48
509			99.9	-4.9	357.19
510			99.9	-3.7	357.89
511			100.0	-2.5	358.59
512			100.0	-1.2	359.30

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CP1 GND 24 1 (ENABLE CP2 2 VCP 3 OUT2B VREG 4 VBB2 SENSE2 MS1 5 MS2 OUT2A 6 19 PAD RESET OUT1A 7 18 ROSC SENSE1 8 SLEEP 9 VBB1 6 **VDD** 10 OUT1B 5 STEP DIR 11 REF 12 GND 13

Pin-out Diagram

TSSOP24



TSSOP24		Pin Description				
1	CP1	Charge pump capacitor terminal				
2	CP2	Charge pump capacitor terminal				
3	VCP	Reservoir capacitor terminal				
4	VREG	Regulator decoupling terminal				
5	MS1	Logic input				
6	MS2	Logic input				
7	\RESET	Logic input				
8	ROSC	Timing set				
9	\SLEEP	Logic input				
10	VDD	Logic supply				
11	STEP	Logic input				
12	REF	Gm reference voltage input				
13,24	GND	Ground*				
14	DIR	Logic input				
15	OUT1B	DMOS Full Bridge 1 Output B				
16	VBB1	Load supply				
17	SENSE1	Sense resistor terminal for Bridge 1				
18	OUT1A	DMOS Full Bridge 1 Output A				
19	OUT2A	DMOS Full Bridge 2 Output A				
20	SENSE2	Sense resistor terminal for Bridge 2				
21	VBB2	Load supply				
22	OUT2B	DMOS Full Bridge 2 Output B				
23	\ENABLE	Logic input				
_	PAD	Exposed pad for enhanced thermal dissipation*				

Terminal List Table

*The GND pins must be tied together externally by connecting to the PAD ground plane under the device.



TSSOP 24 with exposed thermal pad





С



Symbol	Dimensions Ir	n Millimeters	Dimensions In Inches		
Symbol	Min.	Max.	Min.	Max.	
A	—	1.200		0.047	
A1	0.050	0.150	0.002	0.006	
A2	0.800	1.050	0.031	0.041	
b	0.190	0.300	0.007	0.012	
С	0.090	0.200	0.004	0.008	
D	7.700	7.900	0.303	0.311	
D1	3.950	4.150	0.156	0.163	
E	6.250	6.550	0.246	0.258	
E1	4.300	4.500	0.169	0.177	
E2	2.750	2.950	0.108	0.116	
е	0.650(BSC)		0.026	(BSC)	
L	0.450	0.750	0.018	0.030	
θ	0°	8°	0°	8°	

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